SRAM FORMED ON SOI SUBSTRATE

Abstract of the Disclosure

An SRAM capable of reducing the overall area consumed by the circuit and capable of improving the mobility and operational characteristics of a PMOS transistor is provided. The SRAM is formed on an SOI substrate having first and second active areas. A first access NMOS transistor and a first inverter, which is constituted by a first drive NMOS transistor and a first load PMOS transistor, are formed on the first active area of the SOI substrate. A second access NMOS transistor and a second inverter, which is constituted by a first drive NMOS transistor and a first load PMOS transistor, are formed on the second active area of the SOI substrate. Here, the channels of the first and second load PMOS transistors extend so that carriers move in a [110] silicon crystallization growth direction. In each active area, the drain (or source) of an access NMOS transistor, the drain of a drive NMOS transistor, and the drain of a load PMOS transistor contact one another in a shared region. Because the SRAM is formed on the SOI substrate, the size of the resulting chip can be reduced. Also, because the channels of the first and second load PMOS transistors extend so that carriers move in the [110] silicon crystallization growth direction, the mobility of the PMOS transistors is improved.

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